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(57) A test access port controller is provided for implementing scan testing with a chain of scan latches on an integrated circuit. The test access port controller can implement a structural test or a performance test. Selection between the two types of test is achieved through logic circuitry of the test access port controller. An integrated circuit and a test system are also provided.

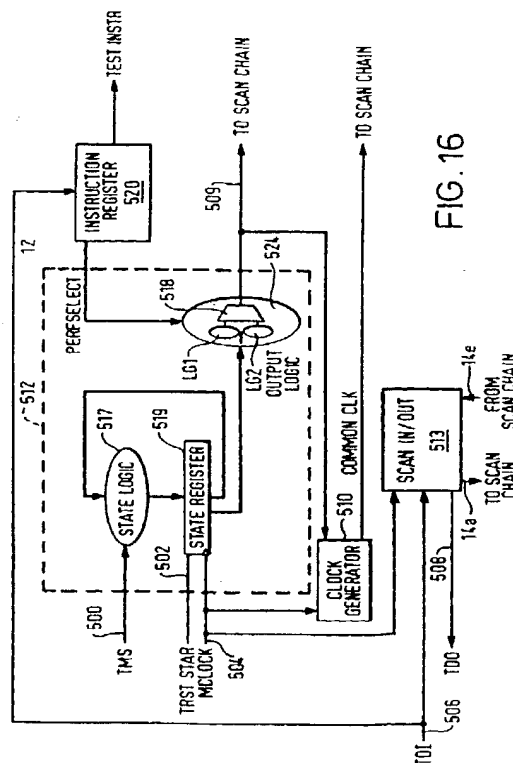


FIG 16

EP 0 702 239 A3

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European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 95 30 5859

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	PROCEEDINGS OF THE IEEE 1992 CUSTOM INTEGRATED CIRCUITS CONFERENCE, 3 May 1992, BOSTON, MA, USA pages 13.2.1 - 13.2.4, XP000340902 H. CHANG ET AL. 'Delay Test Techniques for Boundary Scan based Architectures' * page 13.2.1 - page 13.2.3, right column, line 26; figures 1-9 *	1,9	G01R31/3173 G01R31/3185 G06F11/24 G06F11/267
A	JOURNAL OF ELECTRONIC TESTING : THEORY AND APPLICATIONS, vol.2, no.1, March 1991, DORDRECHT, NL pages 27 - 42, XP000214732 C.M. MAUNDER E AL. 'An Introduction to the Boundary Scan Standard : ANSI/IEEE Std 1149.1' * the whole document *	1-8	
A	EP-A-0 402 134 (TEXAS INSTRUMENTS INCORPORATED) * the whole document *	1-8	
A	* column 35, line 2 - line 15; figure 21 *	9	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
X	EP-A-0 548 585 (INTERNATIONAL BUSINESS MACHINES CORPORATION) * the whole document *	9	G06F
A	AT&T TECHNICAL JOURNAL, vol.73, no.2, March 1994, NEW YORK, USA pages 30 - 39, XP000445588 V.D. AGRAWAL ET AL. 'Built-In Self-Test for Digital Integrated Circuits' * page 34, right column, line 9 - page 35, left column, line 24; figures 1,2 *	9	
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 19 January 1996	Examiner Absalom, R
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	
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